

CADENCE SPB/OrCAD RELEASE 16.3 README -- Windows Version

Installation Guide

You can find the *Cadence SPB/OrCAD 16.3 Release Installation Guide for Windows, Version 16.3* (pcbInstall.pdf) in the Documents folder of the Disk 1 folder of the Cadence Product DVD.

Migration Information

Important migration information is contained in the *Migration Guide for Allegro® Platform Products Release 16.3*, which is available when you install this software or on Cadence Online Support (<http://support.cadence.com>).

NOTE: OrCAD customers need to contact Cadence Channel Partners. Cadence Channel Partners are listed at: http://www.cadence.com/Alliances/channel_partner/pages/default.aspx.

System Requirements

Information about minimum and recommended system requirements can be found in the Documents folder of the Disk 1 folder in the *Allegro Platform System Requirements* document (pcbsystemreqs.pdf) or on Cadence Online Support (<http://support.cadence.com>).

NOTE: OrCAD customers need to contact Cadence Channel Partners. Cadence Channel Partners are listed at: http://www.cadence.com/Alliances/channel_partner/pages/default.aspx.

What's New

Product release notes are available at:

<http://support.cadence.com/wps/mypoc/cos?uri=deeplinkmin:DocumentViewer;src=pubs;q=landing/spb163/prodList.html>

KPNS

The Known Problems and Solutions (KPNS) document is located at:

<http://support.cadence.com/wps/mypoc/cos?uri=deeplinkmin:DocumentViewer;src=pubs;q=landing/spb163/kpnsList.html>

Allegro® /SigXplorer® ABIML Libraries for Default Trace Models with Surface Roughness Effect

The Allegro /SigXplorer ABIML Library is a free library that includes ABIML libraries for SigXplorer default trace models with surface roughness effect. It is designed to provide accurate trace models in Allegro /SigXplorer without time consuming EMS2D solver runs. The libraries can be found at:

<http://www.cadence.com/products/pcb/pages/Downloads.aspx>

This ABIML library is provided free of charge for use with Allegro and SigXplorer. The library is provided as a zipped archive, with installation instructions included.

Custom Environments

Customers using custom batch files or scripts to set up their environments must add the following to their path. There is the potential that some Allegro products may not launch without this setting.

%CDSR00T%\OpenAccess\bin\win32\opt

Downloading and installing SPB Software

Cadence software can be downloaded from:

<http://downloads.cadence.com>

NOTE: OrCAD customers can contact Cadence Channel Partners to obtain their software.

Cadence Channel Partners are listed at:

http://www.cadence.com/Alliances/channel_partner/pages/default.aspx.

Download Disks 1 through 3 and then extract the zip files into a temporary directory such as `cdntemp`. This will leave you with a directory structure that looks like:

```
Disk1 folder
Disk2 folder
Disk3 folder
autorun.inf
setup.exe
setup.ini
```

Complete the installation by running `setup.exe` from the temporary directory or consult the installation guide for more detailed information.

WARNING: The installer will automatically add the programs in this release to the Windows Firewall Exceptions list for Windows XP and Service Pack 2 at the end of the installation process. If you do NOT want the installer to do this, you must run `setup.exe` from a DOS command prompt window with the following switch:

```
setup.exe -nofirewallexceptions
```

When the license manager installation is complete, continue by installing the Cadence products.

NOTE: If you are prompted to reboot, reboot the machine and log in with the administrator privileges login id to successfully complete the installation.

List of Fixed CCRs

- [Enhancement CCRs](#)
- [Bug CCRs](#)

Enhancement CCRs:

CCR ID	Description
7419	Customer menu options added to Allegro menus
8230	Use via in area constraint does not work
10658	Modify default formatting for Label texts and linewidths
12216	Cannot set color or line width for wires on net-by net basis
13083	flip/mirror design to back side
13373	Select length of pin graphics
18072	Add docking option for probe cursor box.
21451	Change Probe print trace color yellow to alternate.
32798	pxllite complex hierarchy netname enhancement
33896	Option for changing the PSpice probe cursor
39600	Option to see time spent on allegro database
40754	Linux OS support for PSpice
60427	Add different subclasses for pin_number top and bottom
77555	Capability to export PSpice probe data points in csv format
107219	Capture.ini switch is needed as a Registry entry like PSpice
132769	Footprint viewer in CIS should also show pad spacing info
158838	Need easy way to delete marker
159977	need attribute mapping capability in mbs2lib and mbs2brd
162382	Enhance quickplace using schematic page from ORCAD
164790	Improve autorouting quality on diff pair w/match length rule
205909	Constraint Manager displays in Allegro no graphic mode
210027	Delete dynamic shape removes net name from copied vias
222127	PADS_IN: Constraints are not imported with the design.
236698	Report Unused parts in multiple parts package should be DRC
240525	Add ability to change cursor color in PSpice Probe window
245193	export dxf height information when blocks are unchecked
254183	Multithreading for DRC and CM analysis in Allegro
282027	Problem with Split Part and part graphics
282507	request to import IBIS file directly
283698	place by schematic page number window need enhancement
288540	Schematic page# display order request for Quick place
290283	PSpice - Probe - setting background color from UI
290641	Option to copy paste cursor value
298081	Models from Funtion.olb need more explanation
323813	Need negation and exclusion function in ADE reports
341484	Wirebond: Tools to generate wirebond manufacturing outputs
353212	Variant Name is not coming in Standard BOM
360602	Enhancement to Show element on a via
362934	Enhancement for Allegro to utilize Dual Processors.
364850	change the font properties of Label Text
367468	Need a real DML_PATH environment variable
380714	Ability to have Power pin set to Not Connect
382860	Display parts and nets in different colors
384488	Add DEVICE and REFDES filter to Signal Model Browser
391487	Ability to have user defined directory for storing distribution files for MC analysis
420008	The renamed differential pair names are different in CM of ConceptHDL and CM of Allegro.
420023	It should be possible to Delete a differential pair defined by SIGNAL_MODEL (.dml) on CM.

420648	Need to get RF Elements to retain previously entered values
429280	ARC is unable to load/save rules - submitted for tracking with Medtronic SiP benchmark
430549	GUI for ADRC XML Rule files
430558	Store last used ADRC rule check ini and check values in .sip database
452606	Can we have last plot as a default
454452	Allow neighboring/overlapping die pads on same net to go to same finger during wirebond add.
456854	full AMS Simulator menu without pspice.ini in registry
464056	Setup option to always prompt to baseline a new part
469378	Enhancement : Hide/Unhide feature for trace
475077	Schematic Generation Setup form is missing the Port symbol selection. It was there in the 15.7 release.
475714	User Guide should mention that Temp Sweep is not honored in AA Flow?
480843	Requesting ability to View > Zoom Mirror current view.
484632	Request for Bond finger to snap to Guide in Free placement of Bond pads
490948	Provide a sketch line and text property form
500550	CRef's should be preserved with the next run of the schgen in the preserve mode.
505284	Enhance The ConceptHDL can set the color for \$XR0 property.
512748	improving arc routing
513967	staggered C-line via arrays
515333	Option to specify spacing between Components in the Generated Schematic
524924	Add PSpice enabled part gnd to standard library folder
525748	Why is MC Analysis Sigma value 1/3rd of 15.7 version value?
526818	Retain Hard Packaging Information option does not work for SECs.
528391	SigXplorer measurement is wrong
533844	Allegro password not encrypted in the .brd file.
536681	In the ADRC tool requesting a "Layer" option for Conductor to Package Substrate Edge Spacing
536948	Allow sorting of power symbols
539407	In ADRC Minimum Shape Check requesting individual "Layer" option
541145	slide command does not support to keeping the existing arc
541214	about supporting OpenDrain Model in Quad2signoise
542414	A function to force diff pair spacing to primary gap.
542803	A "Minimum Shape Check Soldermask" entry is needed in ADRC
543470	Provide rectangle and line width thickness for Drill legend in NC drill Param
543766	Crefer fails to annotate occurrence properties to offpage symbols in replicated blocks
545408	Cursors are toggled off when deleting a plot
546891	Enhancement: message improvement when expand design action in Concept
546985	XOR function to allow to compare layers within different or same designs
548920	Add a document of which properties can be synced and which cannot be and the files required
553669	Add a 3D viewer to Allegro
555183	Wire Bond Report --- Report field should have save function for reuse
556200	Need listing of DE HDL command names and switches.
556883	Grid point for Origin to be highlighted
559638	Enhancement for importing height from PADS in allegro
559724	Request cline via arrays to be applied to diffpair nets
560134	Show Element Customized Display
563957	Enhance Color Dialog form Class/Subclass section to expand vertically when the form size increases.
568058	Request to have component information available through the context menus
568273	documentation of variables in Capture.ini
569615	Enhancement to import constraints from Mentor Board Station to Allegro PCB
569680	BOMHDL defaults to the wrong file type when html report type is selected
569784	Request ability to assign netname to via during copy
569863	User would like to set a larger default trace width
570128	Enhancement : Packager setup for subdesign drop down
570195	SiP - Provide option to create/combine BF labeling with additional text required for Bond diagrams

570861	Unconnected mark does not be removed even after wire is connected to the pin.
575211	Web links in CIS explorer are not working when Firefox 3 as a default Browser
577944	Enhancement request to have the drill legend for thru holes and slots to be separated without being on top of each other
583630	Can Multiple Section pop up box be disabled?
583712	Ability to have string values for SCHEMATIC_GROUP property
585904	Find a schematic page with help of nets
589316	Document change in Gaussian distribution for PSpice MC from 3 sigma to 1 sigma
589512	RF component snap is 'too clever'
590246	CIS to Allegro flow to include or ignore constraints same as HDL to Allegro
591306	Suppress RF edit window when changing RF Element properties
591318	Use RF setup values or retain changed values in RF Element forms
591443	Temporary highlighting is lost when using the Copy command
591450	Provide a dynamic tapering option to RF PCB Route
591489	Would like to suppress RF Snap windowing around the user pick automatically
591812	Provide move options for the RF Snap command
591817	Provide easy group and element ID in repackage form
591825	Quickplace for RF Elements
591865	Request for more information on 'Other' Netlist formats
596392	Publish PDF needs improved error messages for missing installation.
596555	Request alias symbols documentation to include and clarify when necessary to rotate 180 degrees
596843	Cannot do global search after importing read-only schematic block
597808	Option to increase the default thickness of all traces in Probe
599499	Plotting from within Allegro does not find path to stipple file
604125	Manufacture>Create Bond finger Soldermask.
605023	Need rats by layer function for Free Viewer
605112	Dies should not be counted as conductor layers in Design Summary Report of SiP
605373	importing and Exporting BondWires
609035	Voltage_bus part - Make pin number invisible
609561	Enhance Circuit Replicate to support coppers shapes connect lines and vias
610934	Retain user input values in RF PCB forms
612008	Mirror Rules need to be documented for axlTransformObject.
613639	Update Documentation for "split_inst_name" property.
614345	Email facility for Design partition on Solaris does not work
615139	option DMFACTOR documentation missing in pspcref.pdf
615374	Retain Soldermask Thickness value in 3D Viewer Options
615850	Auto Setup should honor device setup parameters if component value is null
615988	PDV When importing from Mentor does the browser not remember the last location of import
616529	15.7 Design Entry HDL fails with Out of Memory message
616873	Uppercase characters in design name error should be improved
617976	Enhancement for a way to sort user subclass in define subclass form
620289	Server 2003 support information in pcbsystemreqs.pdf
620303	Enhancement: Shortcut key for "Select Entire Net"
621054	Renamed net in netlist isolates components from the rest of the net.
621955	Offset Via Generator utility should show a warning message if vias are already present.
622203	Requesting that "DFA Constraint Spreadsheet" icon be added in Customization >Toolbar commands
623218	display pin names associated with a net in net Properties
623908	Mirror Symbols while dynamically moving enhancement
624817	Display padstack name in data tips when hovering over Pad-stack
625733	In Netlist Report they are requesting square bracket vs angle bracket
626605	Extract topology with routed interconnect to include via's in Allegro DesignPlanner, PCB XL and PCB GXL
626673	16.2 Die Stack Editor - Add option for DIE x y cords within DIE STACK form - shows rotation and allows move but
629008	enhancements for find command
629548	Request an Option in Create Plating Bar where it may be directed to a different Subclass

630949 DRC for bond wire to bond wire requires additional parameter "wire profile" to "wire profile"

630955 SCM does not see design difference after update of fixed die/BGA in cdnsip

630973 SCM should see the net assignment made in CDNSIP for Power and Ground pins

631609 Clarify how to generate a cref.dat file in Cadence Help

631697 Want to degass many shapes in succession with custom parameters

632754 pspPN and lib_list should reflect location of new models in 16.2

633440 Sensitivity not varying components correctly

633842 Add note to docs regarding padstack quickview

634350 Enhancement suggestions for pop up info boxes.

634877 Export netlist with properties changes scope from global to local

635118 SKILL variable to obtain list of Classes and user defined subclasses in a database

635233 Place hierarchical pin tool tip

635543 Any command to get the current line/lock type information?

635579 Enhancement for Structured format in parameter file

636930 Die Export option to create symbol either from schematic or layout

637195 Allow for SKill access to backdrill info on padstacks

637768 Enhancement to assign different colors to different net based on a unique property

638455 Enhancement: Add some details regarding nomd.lib

638581 ENH - Press ESC button Spreadsheet window disappear

638622 Add note to CM Spacing Domain Region worksheets regarding shape2element clearance

638910 Enhancement to sort the list of available vias alphabetically in the via list ?

639630 Does the Net_Short property work with Modules?

640262 Request object membership count in the status line and forms of CM.

640280 Provide resizable windows in CM and other apps

640668 File>Change Editor needs ability to go from GXL to Performance L or Design L.

642095 Ability to disable the Pop-Up description of elements

642298 ENH: For license checkout detailed message

642422 After Copy parameters from one part to other in partmanager forgets previously highlighted line

642865 Allow format of hyperlinks in ptf files

642894 ERROR(SPCOCN-1993) is not documented anywhere in Cadence Help

643381 Add an option to ts2dml to allow user specified port ordering.

643390 Request for a switch or button that would allow Properties to be maintained during a shape merge

643625 Bond Wire export to DXF does not support WYSWYG

643790 Include Associated Components in the Verilog netlist

644216 Store Filter Row Data and Units Of Measurement in site-specific file.

644248 Need a better solution to identify and handle unstuffed components

644350 Incorrect upper/lower case for axlPadstackToDisk in Allegro SKILL reference manual

646662 Enhancement to add feature to toggle on/off inter communication tool from within PCB Editor when using DE CIS.

646981 about the treatment of NO_GLOSS property in Missing Fillets Report

647480 global setting for adrc settings in sip via techfile

647617 Degassing not suppressing shapes less than size specified

648210 Request for Working Layer (WL) model in all tier Allegro tools..

648218 must delete keyword "multiwire" from Doc

648533 The cross probe highlighting between DEHDL and Allegro PCB Editor is not documented

648801 Stream Out issue for SPACER

648930 If two PPT option set names match a given component which one will be used?

649603 about spara import

649607 Management of SiP Technology File and Project Information

649610 Management of Part Table (PTF) Files

649613 Management of Library Lists

651684 documentation improvement request on cross-probing in Capture to Allegro to Constraint Manager

652335 Tooltips clutter Place Part dialog.Option to switch it OF and ON

652511 Unplace Component command

652547 Description of ForceDBArg1 should be added to PSpice Users guide

652554 Enhancement request for Allegro to check the vias used to the allowable vias defined in constraint manager

652939 Is there a way to predefine the values for Sample Start Height and Sample Start Length in Wire Profile Editor?

653027 Explicit RMB "Done" option is required in Part Developer symbol editor when editing text

653359 Setting the \$PN to # does not set the pin numbers to invisible when part is sectioned using the section command

653420 Enhance ADRC rule for Acute Angle Merged Metal Check to work on a user defined minimum constraint value

653471 Request for Die Text In Wizard option to Flip the DIE coordinates

653825 sigxp_tier was not reset when installing a new product suite

653902 Enhancement: Print Option? setting in Capture.ini file

657180 Enhancement: Tooltip for DRC markers

657187 SI model delete enhancement

657189 SI Model assign enhancement #2

657501 Negative planes doesn't match with Film View

659543 Need a Report to show which Die Pins have no bond wire attached

659661 Function needs for setting the rotation angle in finger by group.

661477 Color192 window sections to be resizable

662215 Please add the function of renaming net by batch command.

662325 Skill code example axlDBGetProperties.txt not correct

662982 When you edit shape, minisat should always enable shape

663260 Enhancement: ALG0051 message should be more specific

663754 Enhancement to create Device file when saving dra file on opening another design

664240 Add CNVPATH in User Preferences to place default CNV files

665798 163BETA - provide graphical examples to show result of Flexible Shape Editor actions

666186 Enhancement FishEye functionality in Variant View Mode

666768 Temporary graphics for modules / groups do not reflect true size

666775 Update microvia to microvia DRC markings to avoid upper and lower case confusion

667773 Request for ability to set grid definition by entering simple formula

668110 Customer wants to enter the value of radius when editing routes.

669373 Xnets are not formed correctly in CM. Up to 14 'extra' in a copy of the same design.

669380 Add options for ts2dml in MI

669798 Add all 5 Dyn_Thermal_Con_Type property options to Via_Array.

670775 Request to make the SKILL _axlSetDynamicsRotation and Mirror functions public

671194 Allegro not to crash when opening unsupported files

671337 Request performance improvement to access DML libraries from SigXplorer or PCB SI.

671757 Handling of double quotes in HSPICE subckt.

672930 ERROR [DRC0039] Tap may not be connected with the bus Check Entire net

674666 Report the wirebonds XY coordinates

675118 Cline change width command enhancement

675151 Insert comment option for database elements

675398 RF PCB setup should automatically point at the project file if Allegro is launched from a project manager

675551 schematic to sip layout fail

676814 Signal Library command with Allegro performance license.

676906 Add switch -regenerate_xnets to the dbdoctor dUI

677983 about setting of ibis2signoise option "-d" as default

678036 Request for a Physical design compare.

678798 Identify DC nets command doesn't remove the RATSNEST_SCHEDULE

679926 Testprep fails with no route keepin. Message in testprep.log ambiguous at best

680586 Explanation of functions and macros in online help

682098 Color, font, Text Label in PSpice Probe Window

682695 Offset is outside or on pad edge. DEFAULT INTERNAL: REGULAR-PAD message needs rephrased

682865 When using PTC format IDF files don't use forward slashes.

684409 Add info for non availability of SIGXP on OrCAD Demo version

684713 pin_count view needed for packages

684796 do not delete all vias with DRC for via array

686103	Replace vias evenly spaced apart
686112	Add Connect and Slide keeps cline length
686122	Select objects by polygon
687155	License for batch signoise command
687187	BGA Full stagger matrix wizard generation
687201	Improvement in Find feature
687685	Documentation of new properties in Variables block
688047	Include blank space in pin name as the illegal character in PDV user guide
688830	renaming feature discrete library translator
689720	Need the ability to re-center Vis's in center of Pins when a Die is changed.
695957	master.tag generated from the table design needs to contain the verilog representation of the sch.
696661	Add ability in Offset Via Generator to add vias per a given Net
696812	provide description for axlCnsPurgeAll() skill function in doc
697824	Components not installed of variant design should not be extracted into SigXplorer.
698097	Color Dialog form (color192) does not resize correctly
700262	Unable to add Signal Library Model paths in the Allegro Physical Viewer (part of the Allegro PCB SI -L tool)
700712	Defined pin locations are not used when using Die Text-in Wizard with default option Center pins on symbol origin
701514	axlCNSGetSpacing online documentation enhancement request regarding "bbvia_gap"
701810	Document what all database sources are supported by Capture CIS
702190	Request support of Windows 2008 Server Editions.
702613	Request SaveRefdesModelAssignments support the include original model path option.
703905	Need Hot Fix number Info on Help >> About
704594	Update symbol removes the text present on Package_Geometry/Silkscreen
704899	Split Bundle Methodology Should Include a Next Function
704904	via matrix should be available in Allegro L and OrCAD PCB Designer
705601	Please make listnindex a public Skill command
705615	During Updating Symbol the text location and size are changed so Reset Text location is confusing
706165	idf import fails to expand drawing enough to accept text.
706457	Change type of the fourth optional argument for Mirror in axlGeoRotatePt to boolean
706463	Add optional Character in the starting of each line of the file created by axlLogHeader
706787	Fillet should remain when user slide the segment far from pin/via.
709119	Requesting a pull down menu with "Comp" and "Net" to be added in the Offset Via Generator
711837	remove the comma from the image of grid value separator
714840	Enhancement: Anti-etch can be recognized as Void element.
715454	Option to configure Design Entry HDL for Cadence Help
715713	Enhancement for Wire Short Check during move feature
716671	About the log file of the na2 interface.
717722	Pad designer File > save as should have recent file name in file field
718431	Enhancement request to have DRC checks on negative layers.
719050	Log file should contain username date and time while creating or saving .DRA file
719514	Request length column be added to the Dangling Line Report
720297	about "rip up thermal-relief clines"
722346	DRC checks for mismatches in labeling Net
723661	Add *.pad in the File of type drop down menu when executing QVUpdate
724832	Tackpoint move on a non standard wire bond -> *Error* difference: can't handle (2043.0 - nil)
726057	Request incremental DRC update when enabling DFA constraints.
728908	Add Color View Save and Load in Symbol Editor
729947	User would like a metal usage report

Bug CCRs:

CCR ID	Description
10116	Add Intersheet references does not work in Complex Hierarchy
11833	Junction not automatically placed when it should be.
16310	Simple hierarchy, intersheet refs not referring to H-block
19343	Request for intersheet reference to show grid reference zone
22424	Intersheet refs wont work on imported off-page connectors
34275	Ibis2signoise fails with legal characters in file
85735	Cref annotations of the P_ID+00 Bus were missing
118279	PSpice command line options problem
134692	DDB_WARN: POWER_GROUP prop. not allowed wrongly coming
136260	Problem with netlisting the design in PSpice
199343	Stackup-Aware SigXplorer
207620	Part in MISC2.OLB has incorrect pin out
270347	Changes to AXL SKILL must be Documented.
283839	lm117 dropout voltage is too large
296826	Variant view displays library property
299384	Part rotation resets the text to default position
328647	Replace Cache takes time for network libraries
340323	Dynamic shapes need same tweaks in 15.7 as in 15.5.1 to fill
341035	Dynamic shape fails to fill in design that has cline arcs
390692	Via not getting transferred through the Area Constraint from Allegro to Spectra
405611	Environment variable for SIGNAL_INSTALL_DIR is resolved.
428261	spaces at end of pin name Could not create new pin inst library correction utility
436908	The color dialog window will loose the vertical scroll bar after being minimized.
437369	Menu selection of Export > Libraries fails to issue the dlib command.
462783	Busname is too long
495671	Unable to add the signal stubs due to the overlap between SIG_NAME & VALUE Props.
509393	NC drill legend copies null nc_param.txt to current dir.
512809	Window Prt.part.ptf shrinks by 30% and I have to maximize it.
520802	Global Navigate Zoom to Object needs to remember last setting
528686	During text edit the cursor overlaps a letter rather than in between
531555	The diode BAV99 from library works inverted in compare with the graphical representation.
532603	Specifying TC1 and TC2 properties does not seem to have effect
547339	CM-SigXplorer extraction shows different topology in DE HDL vs PCB Editor
548143	Dynamic shape on Etch TOP will not void properly.
550657	Importing registries do not setup printers from MWcontrol
552227	about die export padstack layer mapping
553035	Cref Synonym and Netsbypage reports do not match netlist
557660	Incorrect value for I_sinusoidal of pspice_elem
558164	All variants are affected by function regardless of being called for
558692	Memory leak problem in loading marker files
565681	Filling in values in CM by using ctrl+c,ctrl+v and arrow keys is not working as it should.
567606	PDV selecting pins in symbol editor shows pins off grid during move
568049	Genview crashes
575353	Large box displayed with place manual-h and no RefDes variable set
581848	not able to edit Padstack Boundary
591847	Add Intersheet References does not work on simple H design.
592381	Physical Min/Max line width values not check on internal rows or forms.
593076	Cannot redisplay an invisible OFFPAGE connector's name
598038	Detail button of Markers window with 16.01
600967	wrong order of nodes in PSpiceTemplate for part AD8138/AD
601415	Allegro Design Entry Tutorial corrections.
601531	When using the place manual command and rotating part a ghost image is left behind

603181	Formula to calculate the Actual Temperature for Smoke is incorrect.
604965	need to document how tcl cmd addComponent handles property values with spaces
605843	Aliased nets do not fully dehighlight when next net is highlighted
606493	Targeted nets are not remaining targets
608150	TestPrep generation is creating DRC errors
608787	Missing Constraints Report
608942	PDF Publisher output misaligns text in tables
612511	Error in Flow Tutorial regarding checking default user units
612982	VLIM model giving error that line is too long
613194	Adding wire bonds with current selection does not yield DRC's, mismatching Allow DRC violations option.
613738	Variant BOM report lists identical parts in separate lines due to POWER_GROUP
617146	Symbol fails to place through Component Browser
617327	Change root operation results in SCM crash
617784	Trying to open page 2 of the design Capture crashes
618150	Property Editor Functionality
618617	Enabling strokes requires checking/unchecking options boxes
618771	PDV error SPLBPD-382 when importing from APD.
619053	Diff Pair problem with creating them in DEHDL.
619849	Hierarchical Blocks Loosing reference
620001	Measurement's Maximum range calculation is not correct
620343	Bogus error during schematic write
620826	Changing the units of dimensions does not work
621072	Capture CIS Crash while configuring Database
621163	Ambiguity about the how is the "start of the wire" defined in CDNSIP for ADRC Wire to bondfinger optical short
622263	Drill Customization sort order for oval oblong slots should account for Size Y
622583	Allegro produces erroneous error msg - symbol not found when the placebound is too large for the board.
622692	Why is VGSR negative for N-channel MOSFETs
624378	Device file content conflict
624492	Model Editor finds the wrong model definition for BAV99
625462	Symbol pins Property are lost when once stretched
625519	hspice_mt is not used in Channel Analysis simulation
626674	Allegro CDS_SITE setting don't appear to match documentation
627018	Find Net in instance mode displays twice
627864	EDIF c2esch crashes
628077	Degas not voiding correctly
628265	no "Unused Blind/Buried Via" Report in APD products
628845	Markers> Packager menu is unselectable even after pxl.mkr is created.
631344	Mouse Wheel Scroll misses the "along with the Control Button"
631792	Design Compare not working for OrCAD PCB Designer.
631910	Capture hangs when working with search option
633084	controlfile for OrCAD installation does not work with PO100E and PO200E
633086	Generate Part for Pspice Model is incorrect
633130	The Verilog netlis is wrong
633223	Running skill from a HDL script causes segmentation fault.
633473	INPUT_SCRIPT inconsistency when removed from .cpm file
634075	draw_etch_outline doesn't work for circular shape/arcs
635779	Allegro OpenGL distorting text at certain zoom levels
636156	Unable to convert SDT Schematic to Capture Design
636215	Allegro documentation for Export Parameters is incorrect
636585	Rotating components in Capture reset property position
636688	Signal Model Assignment UI and Find filter association is broken
636819	Documentation wrongly indicates that DFA Analysis is unavailable in XL
637379	No column for ROOM shown in Constraint Manager
638140	Intersheet References not offsetting relative to Port
638670	Testprep parameters - padstack selections - Bottom Side replacement text not entirely visible.

638987	Change command hangs on customer's database
639052	Database Objects Preventing Layer From Being Deleted report fails to run
639685	Capture crash while deleting a Hierarchical Port from the Design
639698	HOME variable defined with %USERNAME% doesn't use value of variable.
639829	After setting Zoom key(F10) to a new alias Tool Tip is missing the key number
640127	Correct IDF documentation regarding UNOWNED objects
640293	performance issues with scm and large pin count devices
640314	The number of menus written in DE-HDL UserGuide is untrue for Unix/Linux users.
641503	Stop running the VAN check on a PLUMBING body symbol in PDV
641676	Incorrect link to assign refdes help
642053	Drag Connected Objects icon is always display as on
642299	Switch the windows mode by set command
642436	Save As symbol in part editor is not working fine
642713	Materials are not refreshed when material name have only numbers.
642873	Dynamic shapes out of date message refers to Setup Drawing Options
643721	Attributes with Null values in symbol.css files are removed when saved in PDV
643949	Can not create Region-Class-Class for same net class.
644016	APD crashes when creating a tile from LEF file
644733	Import reference text file gives incorrect results
644879	Change forms to enforce naming of lib.defs file
645046	SG1525A PWM model is reporting unmodel pins and producing incorrect results
645427	The save button is not enabled on changing the line width
645996	con2con fails to parse ppt file correctly
646175	Please modify the limit length of "Allegro PCB Editor Limits" correctly.
647555	Drill Customization text Non-standard Drill is not readable.
647628	Annotate Type should be removed from PPT Option set files and documentation
648443	Launching SCM without a license is not reported in debug.log
649166	Capture CIS crashes doing Place Database Part with non-admin User rights
649222	Silent install adds extra License Server to CDS_LIC_FILE on the client
649570	PSpice COM Wrapper error while opening Capture PSpice project.
650558	Die Pad layer changed after refresh padstack
650997	Incorrect Pin Shape in CIS Explorer Footprint window
651000	"Wire length over parent die" violation is incorrect.
651153	Results for imported CSV inconsistent in PDV
651521	Resizing the display color visibility dialog box corrupts the display
651526	Parts are missing in a advance analysis library list document and font size issue
651532	Scroll bars disappear after minimizing the color visibility form
652050	Append waveform does not work in 16.2 for .dat files created in previous release with import text format
652904	significantly low performance issues when using edit interface to delete ports of block
653067	Incorrect warning SPMHNI-198 - Pin name is not legal and will be replaced by ` \$#?
653784	Off-page connector name change to internal starting like "I12345555"
654580	Save As should update lib.defs without executing the edit die operation
656282	BGA Generator adds outline and RefDes to wrong subclass
656723	visibility of clines in 3d viewer needs ALL instead of just CON field in layers
657836	Text crop on User Preferences Editor form
658347	Rule Continuous Soldermask Coverage Check should not work on Cline Segments
659437	Move group fails to display anything with Open GL enabled.
660937	Import techfile fails with etch on layer yet layer has no etch
661369	Importing design fails with the SPCOCN-1158 error when DBL_STR_LEN 'ON'
661754	Hyperlink publish pdf to correct page but wrong grid location
662622	Export Physical reports error Output Layout Filename contains space
662918	Skill code example for axlReportRegister does not work
662971	Moving Bondwires disconnect bondfingers.
663088	Cannot add connect to a C-line in Etch Edit Mode
663220	IMPORT_HFS_HARDSEC_ON_SWAP_PINS directive causes error on save in DEHDL
663726	?Each? menu under RefDes is missing in BOM HDL user guide
664764	Material changes when layer type is changed

664900	Project manager User Preferences Editor form has text crop.
665236	Unable to import a Quartus-II version 9.0 pin file.
665389	Spread between voids not working for customer design
665413	In File> "Import and Export"> "Import-ECO pin table" the NEXT button does nothing.
665451	Import - Part logic - information popup window has incorrect user preferences Editor Category
665661	Wirebond Die Escape Generator failed to generate Clines
666099	Mandating at least one symbol with sizable pins for using size..1(not for size-1..0) SPLBPD-310/SPLBPD-309 on reload
666667	Relational Table View Browsing Issue
667286	import IFF No Component Shape Line Via found in IFF file.
667751	db(v(out)) and vdb(out) gives different results for FFT
668080	Improve handling of curved routes
668081	Capture Crash during Edit options
668393	Dielectric constant or loss tangent values do not update when changing conductor
668785	Capture not displaying variant values for Uppercase Display props
668799	Placing specific part crashes OrCAD Capture
668876	Text on the Add button is crop on the Edit via list form.
668892	Incorrect Parallel Length data in parallelism report
669206	Parallelism rule causing significant performance issues during DRC update
669238	Unable to use permanent highlighting for groups in version 16.x
669323	Allegro PCB SI User Guide Doc page 229 ignoring vias needs to be updated
669336	Error in documentation of DE HDL Reference Guide
670874	getVersion() function not reporting tool version
671811	Allegro extracta fails with more than 10 output files
672420	User defined property added to component instance is a function property in Allegro
672614	translator converts the symbol "\" in the original Spice model to "\""
672615	Translator generates 6 external nodes should only have up to 5 nodes
672618	Translator generates statement in the dml file: Language=hspice causing Spectre run errors
672715	Steam_out takes a long time and then fails but the .log file reports a successful export
673279	Same characters are listed as both valid and invalid in naming rules.
673410	search by net name is finding electrical
674058	Incorrect Variant Report
674291	Library Explorer fails to start and I receive a 'Runtime Error!' pop-up
674555	If the DSN filename contains spaces, autobackup will not write any DBK files to
675192	Adding a second BGA caused dsa_api.c to crash
675231	SiP Layout doesn't handle ! characters in port names from Verilog and OpenAccess.
675562	axlWindowFit() documentation needs to be changed.
675783	SiP Wirebond moving a BF sometimes results in the BF placement on the guideline to become unplaced from alignment option
676201	Cross section impedance not calculating with single license
676601	behavior of launch product from library manager
677582	mirror of die component on sip designs
678013	Error: Symbol not found, though symbol is mapped in psmppath
678427	repeatedly placed symbols has strange instance name
678538	Why derive database does not transfer the Schematic Part property to CIS
678814	Spin a temp group will not rotate the symbol
678851	Difference in lengths in 16.01 and 16.2
678884	dbdoctor fixes corruption and then it's reintroduced
679224	dbdoctor states it fixes an error but the error returns
679960	Capture crashes from diff pair setup menu
680565	Capture dsn files are not properly associated during install
681197	Report generator Hangs Up Allegro PCB Editor
682135	Justification of \$PN placeholders not working in 16.2 release
682204	Cdsserv.exe and cdsqmgr.exe crashes using 16.2 release on Windows
682331	Incorrect reference to the middle mouse button.
683146	export variant path appears wrong in output folder while two DSN are open simultaneously

683182	DRC0037 shows incorrect Alternate Net Alias.
683379	ERROR in Measurement ConversionGain_XRange
684180	Sizable pins and vector pins cannot reside together in a component.
684661	via array created wrong results
684700	via array can not be placed on both sides of the cline
684912	16.2 documentation is incorrect for axlDeleteFillet
684915	Incorrect mention of creating graphics template in the PDV user guide
685685	When the customer tried to merge shapes, they disappeared and do not merge.
686338	ERROR #8012 Database Operation Failed with MS SQL database
686560	Changing pin group property after pin swap resets pin numbers
686736	Load property does not propagate to the associated MECH part
687008	ERROR 8020 after removing Place Icon
687074	Part disappears when you open it
687354	Not able to create allegro netlist 228 ERROR(SPCODD-228): Cannot package
687385	Publish PDF outputs the net name (with underscore) overlaps with wire.
687708	Smoke deration calculations for Capacitor
687715	Getting Warning TJL will not be smoke checked
688606	Inconsistency in synchronization between bias display and icon
689542	Comma in ESpice model name causes simulation failure
690112	Ignored nets are displayed in simulated crosstalk worksheet in CM
691668	Stimulus editor hangs on doing change type
691740	crash when setting coincident uvias in CM beta testing 16.3
694139	Case difference of net and bus while generating FPGA netlist
694716	Waveforms are flat when using IO b-element in HSpice
695109	Incorrect Diff-pair topology extracted by Paksi-E field solver
695431	csv2ptf fails without providing any error message
696273	Shape disappears when updated in CDNSIP 16.01 and not following the constraints
696534	Pin Visibility check box doesn't work while creating part from spreadsheet editor
698494	Shape not getting filled correctly
700160	Error: TVCurve must start at time zero .
700644	Allegro Crashes on doing Zoom In
700725	Create Fanout with Via structure add structure from Top to Int. for bottom pins
701128	Inconsistent warning message : TBreak (Tknee)is less than Simulation Temperature
702557	Incorrect Behavior with FSP 2 FPGA Option License
703324	Cross probing board DRC objects to CM DRC spreadsheet fails to zoom in
704268	remove ARC and TOGGLE rmb options when in add rectangle or add circle command
704317	Capture crash when deleting schematic folder
704475	Allegro SI change editor to Allegro PCB XL causes menu problems
705902	ERROR(SPMHUT-144): Illegal arc specification error when Run DBDoctor
705903	Cannot remove a matrix view after modifying the connections
706169	IDF in error has spelling mistake
706613	Diff pair is not extracting properly through design link.
706729	Import properties fails with ERROR [IMP0020]
708134	Place > Manually command menus not refreshing the Placement list
708145	Creating a netlist with Rev. 57AQ is not formatting correctly
708634	Shapes getting incorrectly displayed in 16.2
710279	ERROR 8020# Place component operation failed.
710859	Unable to create Diff Pair from Autosetup
711739	selecting one component/symbol of class IC can move unrelated component due to incorrect group membership.
712299	Internal application error while creating new design
712898	Netrev should not read PARENT_PPT_PART property value while importing the logic, due to which import logic fails
713465	Problems with dynamic shape creation over routed full-arcs diffpairs
713480	Display issue when adding a custom property to the first bit of the bus.
714072	Error while linking database part
714156	Capture crash while archiving project for external referenced design
716097	Specctra is crash during route.
716212	PACK_SHORT property gives package error for visible POWER pins

717484	Dynamic shape creating voids when moving a symbol
718151	Geometry not selected when we click tab for selection filter in pad designer
720092	Difference of behavior for slide for segments in options tab & RMB options
720191	Delay tune cannot keep the Gap if the diffpair segment is diagonal.
720482	Include steps to Enable PSpice Menus in Design Entry HDL
721415	Two buses are connected without a warning when moved on top of each other
721938	Cross-Section open error
722997	Hyperlink function does not work if zone info. includes hyphen
723146	Pb during compilation using predicate getFileStrings
723159	Typographical Error under "Synchronizing PTF Information" section
723235	client install results in incorrect, redundant, and problematic cds_lic_file variable
724414	State Wins Over Design does not reset the subdesign_suffix block values
724969	Allegro crashes when using place replicate function
725852	Impedance has little difference - BEM2D
726731	SiP - Wirebond -> Edit -> select bond finger -> RMB Change characteristics results in bf not following snap
726763	crash during logic import in Allegro CM enabled flow
727663	Remove Subclass in My Favorites (Color Dialog) doesn't refresh properly
729496	Build error in 16.3 and 16.4 cdnsip.exe